TECHNICAL INFORMATION

SURFACE MOUNT ZERO DEFECT DESIGN CHECK LIST

by John Maxwell
AVX Corporation

Abstract:

Reliable, high-yield SMT assemblies are easily realized if time is taken in the beginning to insure yields and reliability. You cannot slap components down on a PC board with solder and hope for manufacturability; the PC board must be designed to be manufacturable.

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Introduction

Surface mount technology (SMT) has suffered through several false starts, but is now a reality due to circuit density needs. SMT designs are a radical departure from their thru-hole counterparts due to trace/component spacings, size, and sensitivity to processing. It is mandatory that a design be manufacturable in the very beginning as tweeks in the process and rework must be avoided. ZERO DEFECT SOLDERING must be the goal for all SMT designs, and the path starts with the design of the board.

For a board to be manufacturable one must be able to first assemble (place) components accurately and then solder those components to the substrate (PC board) with reliable solder joints, inspect those joints, test the assembly, and finally replace any defective components. Rework, a hideous term which implies constantly fixing a production problem, must be eliminated by design and process control. Only the design aspect will be considered, but proper process control is as important as design for both high yield and reliability.

Zero defect soldering requires proper solder fillet formation. Important factors that determine fillet formation are slightly different between reflow and wave soldering and will be considered separately. Common design factors will be considered as a third category and will include tooling holes, test points, and handling stress.

Reflow Soldering

There are five major sources of induced defects for reflow soldering which fall into two categories; opens or bridges (shorts). Pad design and solder mass present are certainly the most important sources of defects but trace/pad interaction, solder mask design, and component orientation must be taken into consideration to achieve zero defects.

Solder Mass. Excessive solder is the biggest source of chip component defects; opens or drawbridges. Great globs of solder or bulbous solder joints are easy to see or may even be required by the military, but do nothing for strength, increase assembly post solder handling damage, and kill yields with drawbridged chip capacitors and resistors. Also excessive solder can cause bridging between fine pitch IC leads leading to additional rework to fix a production problem.

Surface tension forces exerted by molten solder is the defect generating force of coplanar parts like chip capacitors, resistors, or transistors. It is counteracted by the mass of the part and the moment arm created by the component length and adhesion of molten solder to the opposite end.

Excessive solder or an imbalance of these forces result in a drawbridge or a missing solder joint. Drawbridging is not a problem with just chip capacitors or resistors, but can occur with SOTs (small outline transistors) or even small ICs like an SO-8 resulting in rework.

Inadequate solder is the source of weak or missing solder joints for passive components and coplanarity problems (opens) with ICs. There must be a proper balance between non-coplanar parts like ICs that need more solder than small chip components which require less solder for proper joints and low manufacturing defects. As a side note, the total equivalent wet laydown of solder paste to accommodate both passives and actives should be ≈10–12 mils and must take the board solder plating into account. For example, 3 mils of solder plate is equivalent to 5–6 mils wet laydown of solder paste.

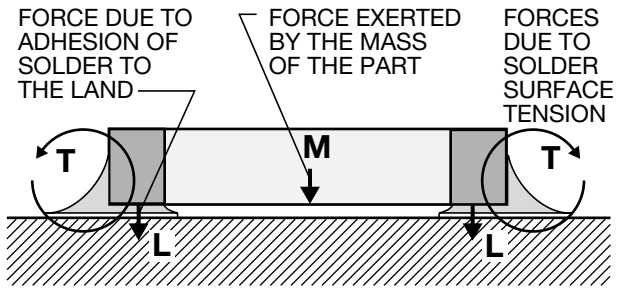


Figure 1. Defect and Counterdefect Forces

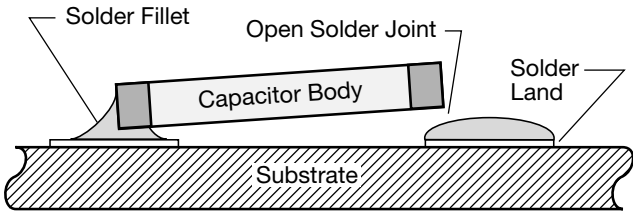


Figure 2. A Drawbridge

Pad Design. Solder fillet shape and size is ultimately determined by the pad design. Unfortunately there is a profusion of recommended pads by component manufacturers, government agencies, industry associations, and component users to name a few; but which has "THE PADS" is the question. Pads recommended by government agencies result in bulbous, easy-to-see solder joints that are neither reliable nor manufacturable. Excessive solder increases soldering defects (tombstoning) and makes components more sensitive to handling damage (cracks). Remember when you sit down for an IRS audit and the agent says, "I'm with the government and I'm here to help you." Would you believe him?

There are a few industry association pad or land pattern and design guidelines that are an excellent place to

start as baseline documents. The most comprehensive set of standards is available from The Institute for Interconnecting and Packaging Electronic Circuits. The guideline of most interest will be IPC-SM-782, "Surface Mount Land Patterns (Configurations and Design Rules)." One thing to remember is that any industry association specification is arrived at through compromise by various members who may have little SMT manufacturing experience. IPC-SM-782 is a prime example of this, many land patterns were established to make it easy to create artwork without understanding the impact on yield. Just now members are doing a study to see if the patterns are usable; a bit late because the specification is in its final form. This is still a good base line document.

The best source for pads is either users or vendors that have reliable, low defect solder joint histories that number in tens of millions. Certain IC and passive component vendors have this history but their pads are different from IPC-SM-782, but no compromise for ease of artwork generation was made at the expense of reliability or yields. Actually small components are more prone to soldering defects than larger parts due to their low mass and small termination surface area.

Pads demand that they have some prior history, are symmetrical, and have been tested in the intended process. Always avoid "Universal Pads" because too much has been compromised. Texas Instruments and Signetics are good sources for IC pads with AVX and Bourns for various passive component pads. Once pads are chosen, test them in your manufacturing process, then thermal cycle and environmentally test the assembly.

Trace Pad Interaction. Connecting traces to pads is one area where thru-hole design techniques are absolutely not applicable. Reflow soldering uses heat transfer from the PC board surface to the pads, reflowing the solder paste on to the component termination. Asymmetry in pad thermal mass results in drawbridges or missing solder joints of low mass components or solder migrating away from a solder joint during reflow. Vias or plated thru-holes present another major problem: capillary action of solder in the via can rob a pad of solder causing a starved or missing solder joint. A few common sense rules are in order:

1) Limit the number of traces entering a pad to a single trace if possible to reduce solder migration.
2) Symmetry is important. Balance the trace entry to a pad to minimize any induced component rotation.
3) No vias or plated thru-holes in a pad: sucks solder out of the joint.
4) Isolate ground planes from components with necked down conductors no closer than 10 mils or wider than 10 mils for passive device pads and no wider than 7 mils for active device pads.
5) Isolate a via pad even further than ground planes due to capillary action. Pad separation should be no closer than 15 mils.

There is a simple test to see if an existing design is manufacturable or to find potential defect sources with a problem board. Screening solder paste on the pads with a stencil and then reflowing the board without components will indicate if there are problem locations. Solder missing from pads after reflow is a prime sign for problems and allows close scrutiny of traces and pads. High yield demands that a board must have uniform solder on pads after reflow or rework will result. Remember, rework is hideous and must be avoided and is counter to reasons for adopting SMT.

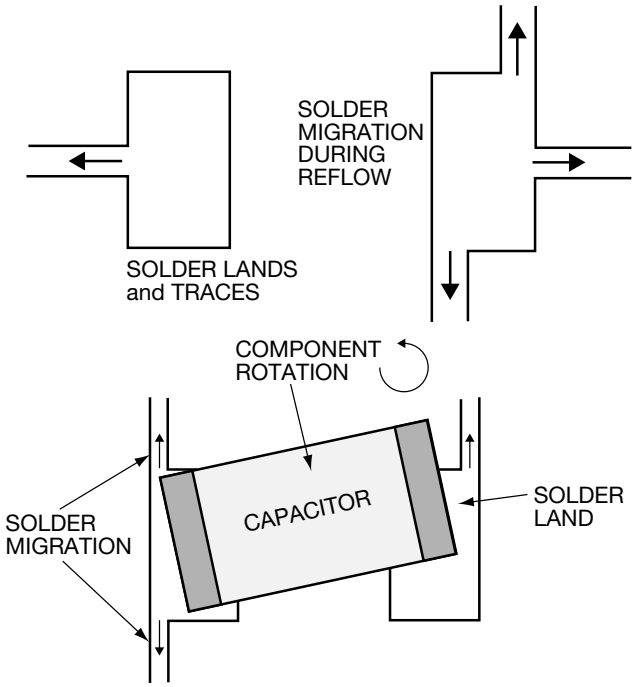


Figure 3. Design Techniques to Avoid

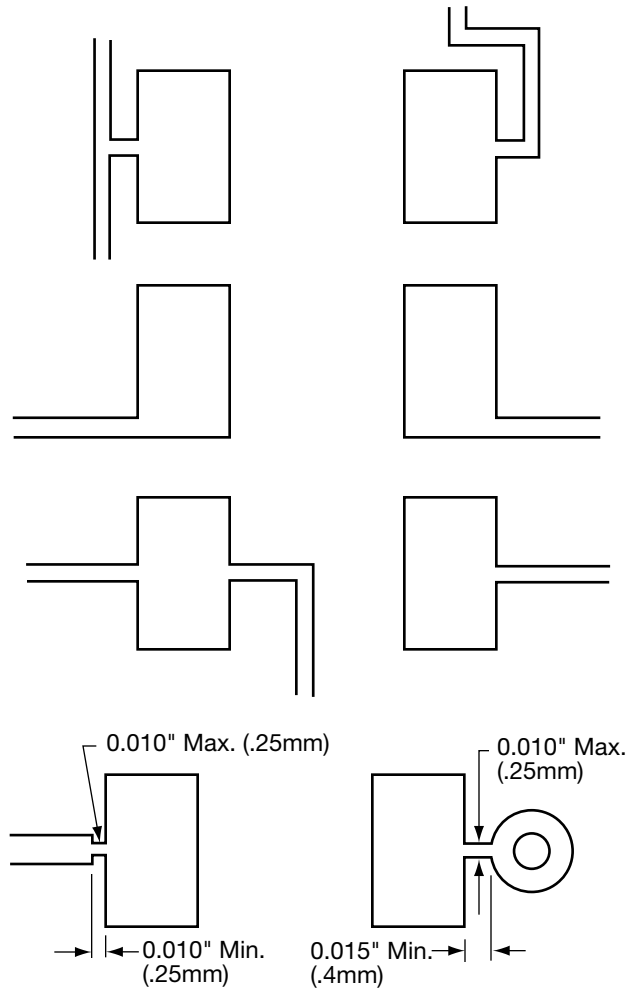


Figure 4. Design Techniques That Work

Solder Mask Design. Again, thru-hole PC board design techniques are inadequate for zero defect surface mount assemblies. Solder mask materials come in many varieties ranging from dry film laminate to screened wet film or photoimagable liquid solder mask. Solder mask thickness ranges from 0.6 mil to 9 mils across mask types. Dry film ranges typically from 3-4 mils, photoimagable from 0.6 to 6 mils across various manufacturers, but is quite tight within a single supplier (i.e., Δs of only a mil) and wet film has the largest variation of 0.6 mil to 9 mils.

Little thought is put into solder mask design for thru-hole boards, a CAD system or artwork house just takes a negative of the pad mask and they are done. Unfortunately improper solder mask design can cause two different types of defects. Misregistration of solder mask artwork or wet film solder mask slump can obscure or contaminate a pad surface causing excessive solder balls or defective solder joints.

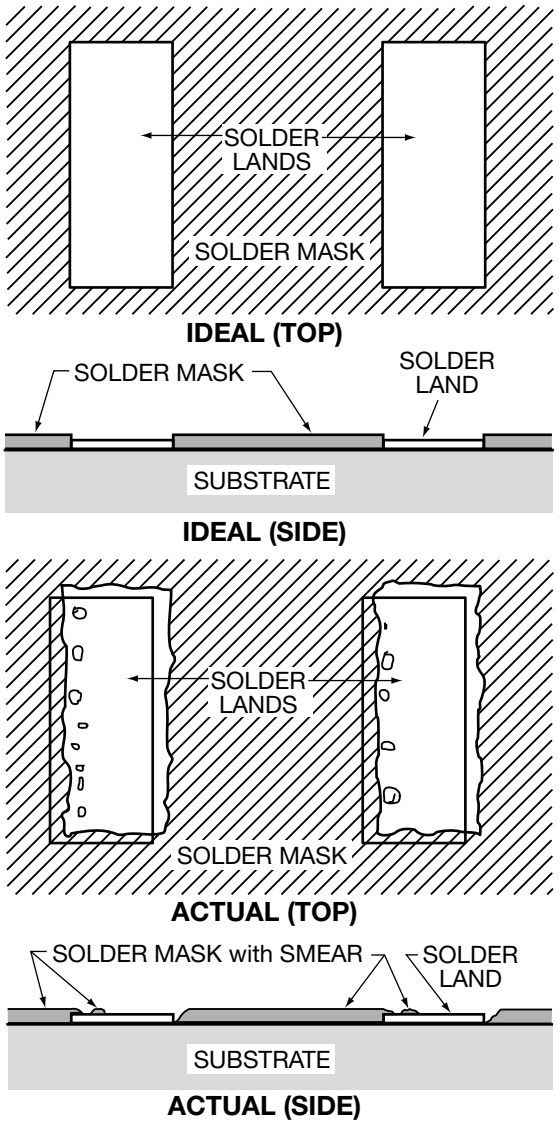


Figure 5. Ideal Solder Mask and the Result

Solder mask artwork should be oversized by 10 mils in each dimension to allow for misregistration or slump, eliminating this source of defects. Solder mask thickness also is the second factor in the elimination of defects. It was found on a production line that when solder mask was too thick, that is solder mask above the base copper pad, exceeded 2 mils, detectable capacitor drawbridging resulted. One ounce of copper is 0.7 mils thick and 2 ounces of copper is 1.4 mils, placing a practical solder mask thickness limit of 3 mils maximum on 1-ounce copper boards and 3.5 mils for 2-ounce boards. These thickness limits are in the middle of dry film thickness range and are much less than many wet film or photoimagable liquid solder masks. Elimination of solder mask between pads removes solder mask thickness problems as a defect source. Using solder mask windows has the added advantage of easier cleaning of flux residues trapped beneath components.

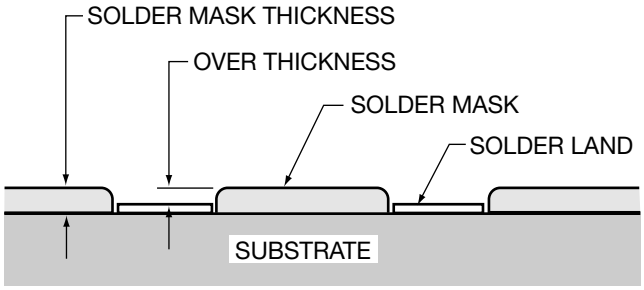


Figure 6. Solder Mask Overthickness

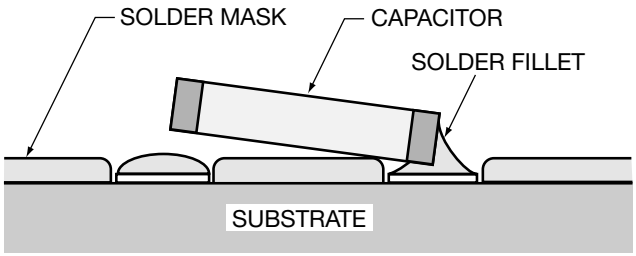
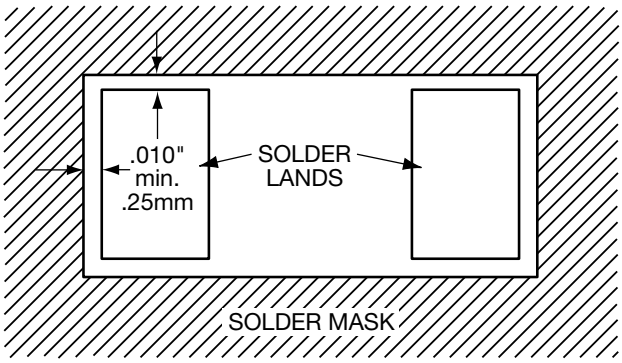
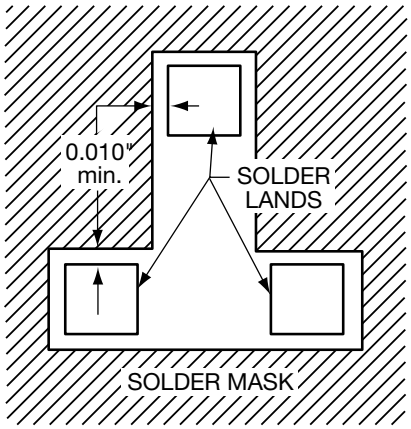


Figure 7. Resulting Induced Drawbridge





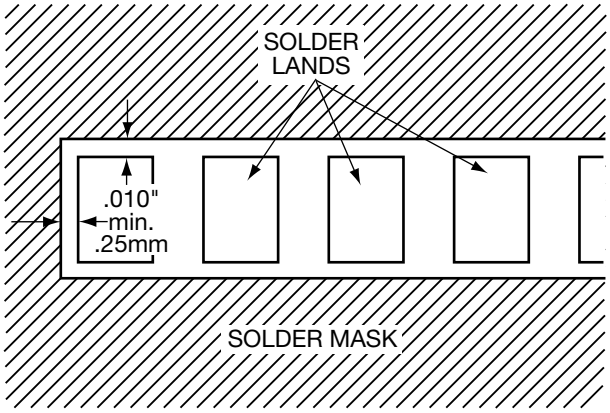


Figure 8. Recommended Solder Mask Windows

You should place solder mask between IC pads when the PC board design runs traces between those pads. This requirement eliminates wet film solder mask totally from consideration because of registration problems. Fine line, high density designs must use photoimagable solder masks because of registration problems.

Component Orientation. Depending on which reflow technique is used, component orientation may or may not be a problem. Ultimately, orientation defects are the result of low mass component termination and differential heating. Temperature rates of rise can be in excess of 50°C/sec. in vapor phase systems with no preheat. This rate of rise is less in vapor phase systems that use preheat but are still substantially higher than infrared reflow soldering. Chip components need to have each termination enter the solder zone simultaneously and low mass transistors and ICs need to enter along their long axis. It is a good idea to have all ICs oriented such that the long axis is parallel to that direction of reflow system belt movement and chip component long axis is perpendicular to that direction for all reflow soldering techniques or excessive tombstoning results.

Wave Soldering

Component orientation, placement, and pad design dictate assembly yields for wave soldering. Reflow soldering uses a deposited solder mass prior to the component placement and reflow operation, but wave soldering is an additive process where the final assembly is run through a solder bath. Proper solder fillet formation is a function of component termination exposure to the solder bath and pad design.

Orientation and Placement. Uniform exposure of component terminations to the solder bath is critical to achieve low defects and reliable solder joints. Simultaneous soldering of opposite terminations is the key for low defect wave soldering. As in reflow soldering, the long axis of chip components must be perpendicular to system belt direction and active components must have the long axis parallel to that direction.

In addition to proper orientation, components cannot be immediately upstream of terminations that are to be soldered or bridges, starved and missing solder joints will result. A gap of 150-200 mils between potential shadow components is enough to eliminate those problems. Component spacing is a different issue and affects both reflow and wave soldering. A small component cannot be in the shadow of a larger one without defects. All component terminations should be parallel in both

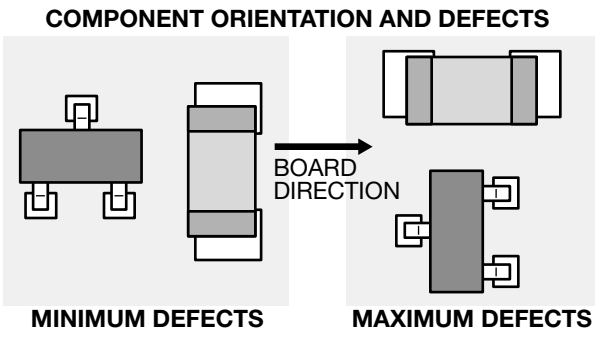


Figure 9. Component Orientation

the X and Y directions and no component should be mounted with an offset angle other than 0° or 90°.

Pad Design. Wave soldering of SMT components is an additive process making pad design absolutely essential for proper solder fillet formation. Bulbous fillets are nice to inspect, but dramatically reduce solder joint life and make the entire assembly more susceptible to handling damage. As with reflow soldered boards, it becomes mandatory to use known good pads and then test the design in the intended process.

Common Design Factors for All Solder Processes

SMT board design factors that have common requirements include tooling holes, test points, component separation, power/ground planes, and post solder assembly stress.

Tooling Holes. The biggest cause of component placement error is improper tooling hole location and diameter accuracy. There are new pick and place machines that use vision to place components on desired pads, but most machines in the installed equipment base do not have this capability, making tooling holes critical in eliminating placement defects by properly registering component pads to the pick and place machine.

Tooling Hole Requirements:

1) Tooling holes must have as much separation as possible with a hole to hole accuracy of ±0.002".
2) Multiple assemblies need tooling holes in both the mother panel and individual boards.
3) Hole size accuracy needs to be –0.000"/+0.003".
4) Tooling holes MUST be referenced to copper artwork datums or fiducial marks with an accuracy of ±0.002" and not referenced to vias or plated thru-holes.

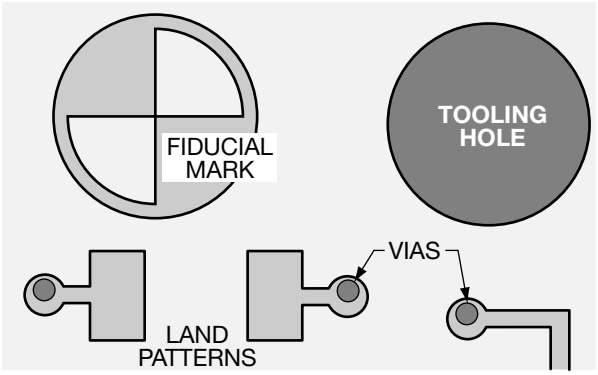


Figure 10. Tooling Holes Referenced to Artwork

Test Points. SMT component terminations and leads must never be probed directly or latent defects will result due to cracking components or damaging solder joints. Test pads for critical nodes that are isolated from component pads must be established.

Test Pad Requirements:

1) Test pads should be on either a 50 or 100 mil grid (100 mil preferred) referenced to artwork fiducial marks.
2) Test pads should be 0.035" in diameter or larger. A 0.040" square pad can be used to visibly distinguish between test and via pads.
3) Isolate test and component pads with necked down traces 10 mils wide with 10 mil minimum separation for passive pads. Use 7 mil wide traces with a 15 mil minimum separation for the smaller active device pads.
4) Never use via pads (plated thru-hole) as test points. Test probes can damage the via barrel/pad interface resulting in intermittent contact after power cycling.

Component Separation. Many factors dictate the component density that you can achieve; pick and place machine accuracy, tooling hole/artwork registration, solder joint inspection, uniform heating during soldering, defective component removal, odd component body sizes, and solder bridging. The following guidelines take these factors into account and have found they result in high yield assembly. It becomes difficult to inspect solder joints or remove defective components when pad to pad or component body to pad spacings drop below 0.050".

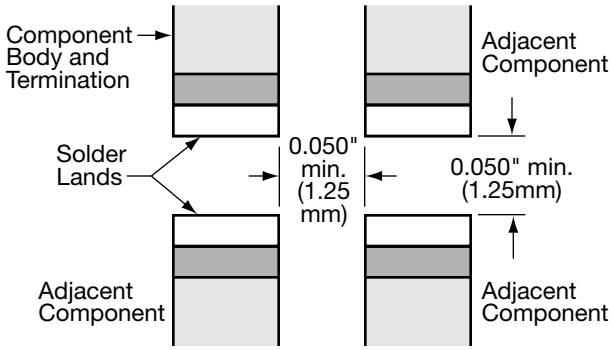


Figure 11. Chip Component Spacing

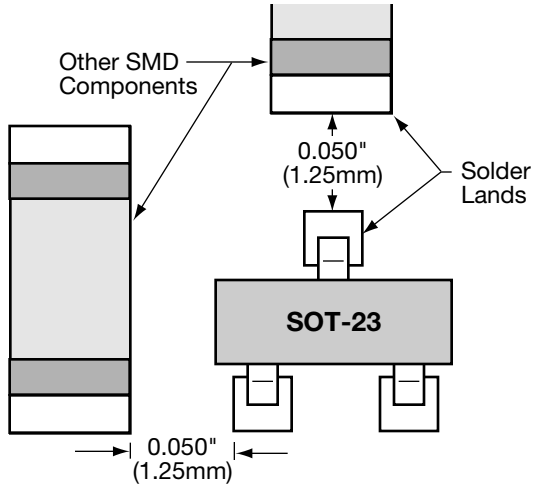


Figure 12. Chip to Transistor Spacing

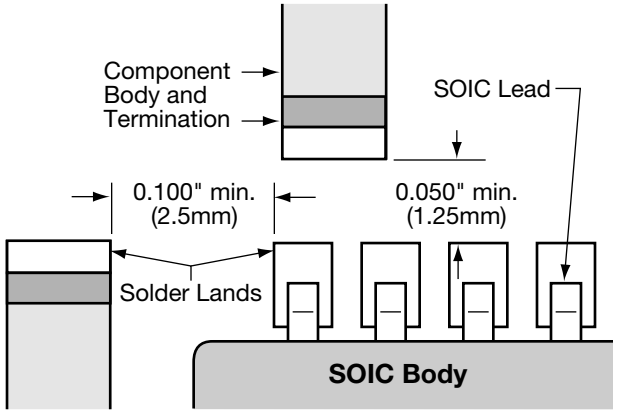


Figure 13. Chip to SOIC Spacing

These spacings can be reduced somewhat with a small sacrifice in yield based on soldering technique and desired component density. Chip to chip and pad to pad spacing can be reduced to 0.025" when reflow soldering is used but is limited to 0.035" for wave soldering due to solder bridging. The same rules can be used for chip to transistors, 0.025" spacing for reflow soldering and 0.035" for wave soldering. Component pad separation can be reduced to 0.025" and 0.035" along the lead side of SOICs, but no reduction is allowed on the end due to body length variations between vendors.

Power/Ground Planes. Copper distribution on both sides of a PC board needs to be as uniform as possible. This is true for any inner layers in multilayer boards. This is to insure uniform heating during preheat and soldering and to minimize board warpage during soldering. CTEs (coefficient of thermal expansion) between copper and epoxy fiber glass and their heating rates are radically different causing board warp during soldering. Board warpage is minimized by:

1) Cross hatching power and ground planes as much as possible.
2) Isolating vias with necked down conductors.
3) Keep metal distribution as uniform as possible on each layer.

Post Solder Handling Stress. Final product configuration should determine initial component orientation and spacing. Little things like testing a board, depanelizing a mother board, installing connectors, or putting it in a chassis are grouped together as post solder handling stress. There are no existing standards that cover how much bending or deflection is allowed before component damage occurs. There are component specifications that cover bending, but depending on dielectric there can be a significant shift in electrical parameters; but no consideration is given to cracking or reliability. Manufacturing and assembly procedures demand that an assembly be handled. Just how much is the question.

The following recommendation is based on manufacturing experience in the elimination of post solder handling cracks. Instead of a linear inch per inch specification which becomes unusable with even moderate sized assemblies, a bend radius was used. This allows for little or no bending in short segments, but relatively large deflection for longer boards.

A bend radius of 60 inches is used to eliminate damage for a broad range of active and passive components. Bend radius allows for only gradual deflection of an assembly along the circumference of a circle with a 60 inch radius. This allows only 0.0084" of deflection for a 1" board segment and 0.124" in 4".

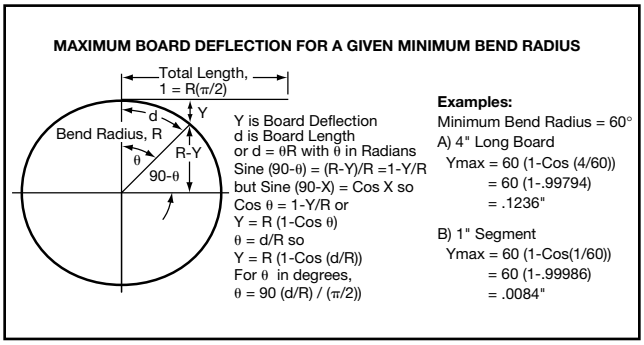


Figure 14. Bend Radius and Board Deflection

There are areas on a board that always experience too much deflection to achieve high yields and reliability. Keep components away from corners and edges because these areas have the greatest deflection and stress. Isolating components from the board edge by more than 200 mils will minimize those problems.

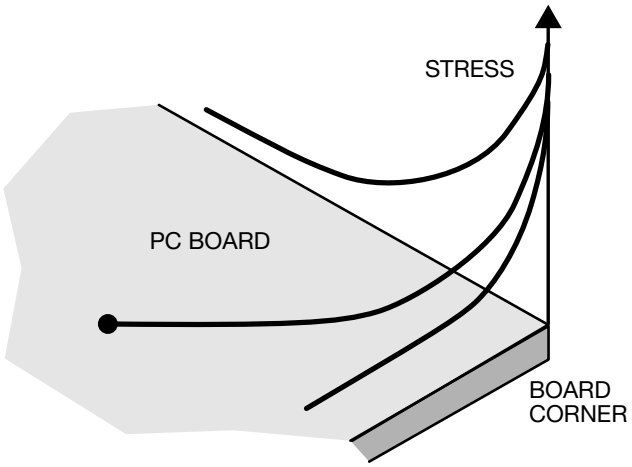


Figure 15. Stress Near a Board Corner

Defects can still occur much further away from the board edge if the board is large and flexible or if components are perpendicular to stress gradients. Components need to be isolated from connectors, mounting holes, pots, etc. to minimize damage from those sources of deflection.

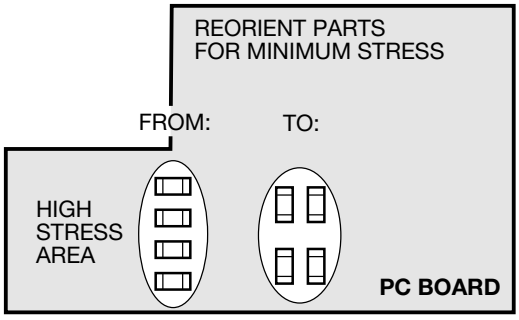


Figure 16. Orient Components for Minimum Stress

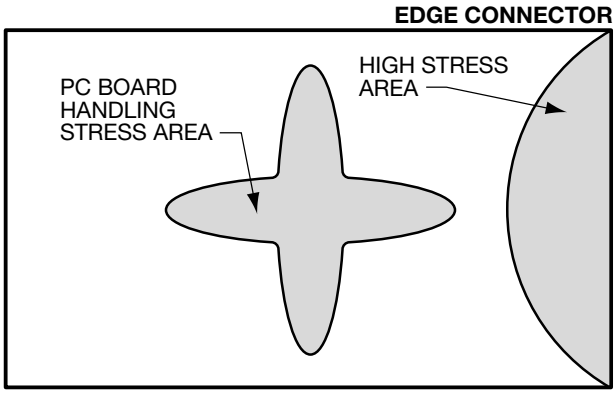


Figure 17. Board Bending and Connector Defect Zones

Some boards are built as a multipanel assembly for mass soldering and then depanelized. Separating soldered boards from a mother board introduces additional stress to components near corners and edges. There are a number of depanelization techniques available; unfortunately, most do not work reliably with SMT assemblies because SMT chip components do not have compliant leads to relieve mechanical stress imparted by the board.

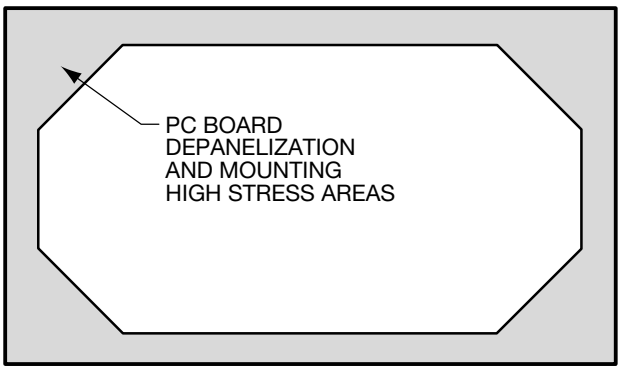


Figure 18. High Stress Areas for Mounting and Depaneling

Reviewing the list, one finds a long one for bad techniques and a shorter one for good techniques.

Examples of bad depanelization techniques—from worst to just really bad:

1) Prescored boards with manual breakout
2) Perforated boards with manual breakout
3) Shearing including blanking shears
4) Routing
5) Breakout tabs, prerouted boards
6) Prepunched boards

Examples of depanelization techniques that do work:

1) High speed fine tooth saws
   a) Use only linear cuts
   b) Rigid fixturing is mandatory
2) Laser cutting
   a) Limited to 0.047" thick PC boards because of excessive charring of board edges
   b) An extra cleaning step due to carbon talc
3) Water Jet
   a) Slow and noisy but the most flexible

Prerouting PC boards prior to assembly can hold board deflection to a minimum, but component defects will still be concentrated near these shear lines.

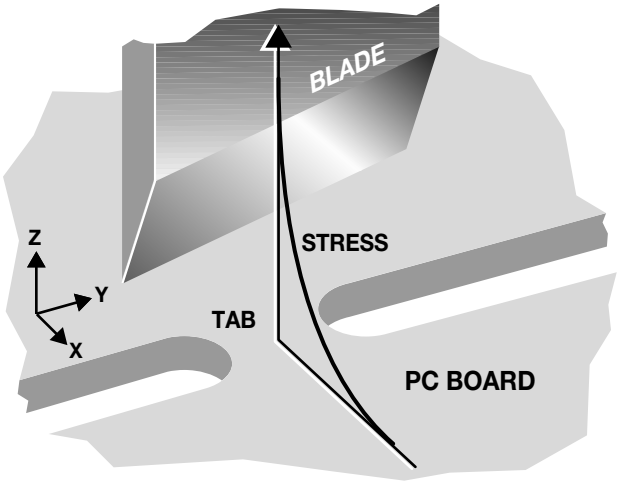


Figure 19. Tab Shearing Stress

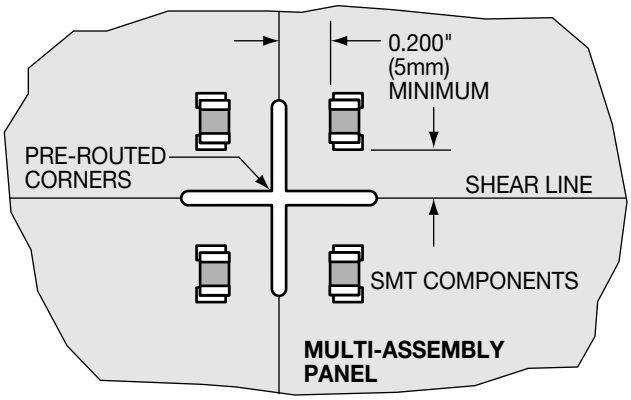


Figure 20. Pre-Routed Corners to Minimize Defects

Conclusions

Reliable, high-yield SMT assemblies are easily realized if time is taken in the beginning to insure yields and reliability. You cannot slap components down on a PC board with solder and hope for manufacturability. Before a design even gets to production, it must have the following:

1) Proper solder fillets
2) Process tested pad designs with no "Universal pads"
3) Trace/pad interaction must be right
4) Proper solder mask design
5) Proper orientation for soldering
6) Proper tooling hole locations and accuracy
7) Testability
8) Uniform metalization on all layers
9) Cross hatched power and ground planes
10) Components isolated from high stress areas
11) Prerouting of corner areas for depaneling

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